Lecture Notes in Management Science (2016) Vol. **8**, 101–105 ISSN 2008-0050 (Print), ISSN 1927-0097 (Online)

Simulation analysis of operational control decisions in semiconductor wafer fabrication

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Proc. ICAOR 2016
Rotterdam, The Netherlands

Keywords:
Batch loading
Bottleneck
Dispatching
Lot release
Semiconductor wafer fabrication

Abstract

This paper examines operational control decisions in a semiconductor wafer fabrication line, including lot release control, dispatching and batch loading. In most previous works, these control problems have been considered separately. In this paper, we consider these problems at the same time, and present new control rules for bottleneck stations, non-bottleneck stations and batch processing stations, respectively. Simulation experiments are carried out to examine the performance of the control rules. Some insights on the performance of the control policies are discussed.

Introduction

In semiconductor wafer fabrication systems (wafer fabs), circuit layers are repeatedly built on wafers by a variety of processes including cleaning, oxidation/diffusion, photolithography, etching, deposition and ion implantation. Each wafer lot (often consisting 25 wafers) visits 300-700 process steps on hundreds of different machines. Because of the long sequences of operations required for the wafers, most wafer fabs suffer from high work-in-process (WIP) inventory and long lead times (about one month). In addition, the cost of building a wafer fab is enormous, often requiring more than ten billion dollars (Ham 2012). Hence, it is very important to achieve high productivity by utilizing resources in an efficient and effective way.

This paper addresses operational control problems in the wafer fab. In most memory chip wafer fabs, the major objective of operational control decisions is to minimize production flow time while maintaining target throughput rate. The control problems in the wafer fab can be classified into two problems, lot release and dispatching. The lot release involves a fab-level decision that determines when and how many wafer lots should be released to the wafer fab while the dispatching is a workstation-level decision that determines which lot should be loaded next on an idle machine. Most of the research works on operational control problems in the fab studied so far address the input release and dispatching problems separately. This paper considers these control problems simultaneously. We present new control rules for bottleneck stations, non-bottleneck stations and batch processing stations, respectively. A simulation model is constructed where all the control policies are incorporated. Through simulation studies, the performance of the presented control policies is evaluated, and some insights on the performance of the control policies are discussed.

Problem description

The control decisions we deal with include dispatching for DP stations, dispatching for BP stations and lot release. The dispatching problems in a wafer fab can be divided into two, sequencing for discrete processing (DP) stations and batching for batch processing (BP) stations. BP stations process a number of wafer lots simultaneously as a batch while DP stations process wafer lots individually. We present control policies for DP stations and BP stations, respectively.

Dispatching for DP stations

When a machine completes processing a wafer lot and there is more than one wafer lot waiting in its queue, a decision is made which lot should be loaded next. Most of the existing dispatching approaches are based on priorities. The priorities are set by using product information such as FCFS(first come first served), SRPT (shortest remaining processing time) and EDD (earliest due date) as well as system status including workload and WIP level. A wide variety of dispatching

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policies have been studied, and they are reviewed extensively in Sarin *et al*. (2011). According to the Theory of Constraints (TOC), the performance of a manufacturing system is mainly determined by its bottleneck resource. Hence, the bottleneck machines often tightly scheduled while the non-bottleneck machines are controlled by using a simple dispatching. In this paper, new dispatching rules are presented for both bottleneck and non-bottleneck stations.

Dispatching for non-bottlenecks

Dispatching for the non-bottleneck machines have been ignored by the research world whose focus is usually on bottleneck stations. Most existing control decisions in non-bottleneck machines use a simple control rule like FCFS rule. Here, we present FCFS_BM (bottleneck machine) and SRPT_BM rules where the decision is made in the way that the downstream bottleneck stations are not starved. In these rules, the control decision is made with FCFS and SRPT rules, respectively, in an ordinary situation. However, if the downstream bottleneck station of a wafer lot is expected to be idle shortly, the wafer lot is loaded with higher priority.

Dispatching for bottlenecks

FCFS_BM and SRPT_BM described above can be used for bottleneck stations. In the wafer fab, it is important to produce the products evenly over time because the large fluctuation of the production amount may result in high finished goods inventory or stockout. We additionally present LOOP_LVL rule for the bottleneck machines. In LOOP_LVL, a target WIP is first calculated for each process loop. Here the process loop is defined as a series of processes between two bottleneck stations. Average and variability of WIP level are obtained through preliminary simulation experiments and used to calculate the target WIP level for each loop. A wafer lot with lower actual/target WIP ratio has a process priority.

Batch loading for BP stations

Batching loading involves the dispatching decision on which product type and how many lots to process next in the BPMs. The commonly used batch loading policy is minimum batch size (MBS) rule where a batch of wafer lots is loaded when current batch size in no less than a predefined MBS. Extensive review on batching decisions is found in van der Zee (2003) and Koo & Moon (2014). In this paper, we present a batch loading rule, MBS_BM, where downstream bottleneck stations are considered in loading decision. In MBS_BM rule, the loading decision is made with MBS rule in an ordinary situation. However, if the downstream bottleneck station of a wafer lot is expected to be idle shortly, the wafer lot is loaded with higher priority, even with batch size less than MBS.

Lot release

The lot release rules can be classified into open-loop release policies and closed-loop release policies. The open-loop release policies release wafer lots into the fab based on a static production schedule regardless of the current system status. One of the simple open-loop release policies is DETERM where wafer lots are released into the fab in a constant interval. The closed-loop release policies consider wafer fab status in release decision making. A simple closed-loop release policy is CONWIP (Spearman, *et al*. 1990) where a constant number of WIPs are maintained in the fab. The other widely known closed-loop release policies include workload regulating (WR) rule (Wein 1988) and starvation avoidance (SA) rule (Glassey and Resende 1998). These two rules consider bottleneck workstations in the fab. It is widely recognized that the closed-loop release control outperforms the open-loop release control.

Simulation analysis

To examine the performance of the operational control strategies, simulation experiments are carried out on a wafer fab. The configuration of the wafer fab is obtained from Wein (1988) with a slight modification. The fab consists of 24 single or multi-server workstations subject to unscheduled facility downtime. Each wafer lot has a process flow with 172 operations at 24 different workstations. There are four batch processing workstations. All the wafer lots visit the bottleneck workstation (workstation 14) 12 times whose utilization is 91.9%.

Table 1 shows the control rules considered in the simulation studies. For lot release rules, a open-loop control policy, DETERM, and two closed-loop control policies, CONWIP and WR(workload regulation), are examined. The parameters for the closed-loop control rules are chosen through preliminary experiments so that the average throughput rate would correspond as closely as possible to the average throughput rate of the DETERM rule. A set of control rules (DETERM, FCFS, FCFS, MBS) is considered as a base case. In this 4-tuple (r1,r2,r3,r4) control rule, r1 denotes lot release, r2 dispatching for non-BM, r3 dispatching for BM, and r4 loading for batching machines. The simulation runs are repeated 20 times for each of the combinations of control rules. Each simulation experiment runs for two years. The statistics from the second year are used for analysis to see the system performance in a steady state.

Table 1. Operational control policies

Control		*Rules*
Lot release		DETERM, CONWIP, WR,
Dispatching	Non-BM	FCFS, SRPT, FCFS_BM, SRPT-BM
	BM	FCFS, SRPT, FCFS_BM, SRPT-BM LOOP_LVL
	Batch	MBS, MBS-BM

From the simulation experiments, we find some more interesting insights on the effect of the operational control decisions on the system performance. Our discussion will be given in the form of answers to the following questions.

Are the proposed control schemes considering bottleneck machines perform well?

In order to evaluate the proposed control schemes where the workload of the downstream bottleneck station is taken into account, the experiments are performed with different control rulesets. Table 2 summarizes the results of different control schemes. Among two important performance measures, throughput rate and lead time, only lead time is compared because the throughput rate is deterministic in DETERM lot release rule. The results show that a set of the proposed control schemes, RA0, provides better performance (less lead time) than the base case. The lead time is reduced by 22.7 hours (almost one day) from 816.4 to 793.7. When we take a close look at the result, we find that dispatching for the bottleneck machine has little effect on the performance (See the result of RA2). It is also found that the batch loading decision at the BP stations has greater effect on the performance than the dispatching decision for the DP stations.

Table 2. Simulation results

Ruleset case	Lot release	Dispatching for Non-BM	Dispatching for BM	Loading for batch processor	Lead time (hours)	Throughput rate(lots)
Base case	DETERM	FCFS	FCFS	MBS	816.4	728.1
RA0	DETERM	FCFS_BM	FCFS_BM	MBS_BM	793.7	733.0
RA1	DETERM	FIFO_BM	FCFS	MBS	807.7	733.5
RA2	DETERM	FCFS	FCFS_BM	MBS	817.0	732.2
RA3	DETERM	FCFS	FCFS	MBS_BM	795.4	731.0

Does input control decisions have more effect on system performance than dispatching decisions?

Many research works insist that the system performance is more strongly affected by lot release rules than dispatching and batching rules (Wein 1988, Li *et al*. 2014). However, our experimental results given in Table 3 tell a different story. Compared with the base case, bottleneck-focused dispatching rule set, RB2, reduces the lead time by 22.7 hours from 816.4 to 793.7 while the closed-loop lot release rule, RB1, reduces the lead time by 20.0 hours from 816.4 to 796.4. The results say that

the dispatching rules have no less influence on the system performance than the lot release rule. It is believed that the importance of the lot release rule becomes less important for the system with very long process steps in the wafer fab.

Table 3. Simulation results

Ruleset case	Lot release	Dispatching for Non-BM	Dispatching for BM	Loading for batch processor	Lead time (hours)	Throughput rate(lots)
Base case	DETERM	FCFS	FCFS	MBS	816.4	728.1
RB1	WR	FCFS	FCFS	MBS	796.4	728.2
RB2	DETERM	FCFS_BM	FCFS_BM	MBS_BM	793.7	733.0

Which one is more important, dispatching for non-bottleneck stations or for bottleneck stations?

Most existing studies on dispatching decisions focus on bottleneck stations (Kim *et al*. 1998; Lee *et al*. 2002). However, the experimental results given in Table 4 show that the control at the non-bottleneck stations have a great influence on the performance as much as control at the bottleneck stations. In fact, it is seen that the control at bottleneck stations have little effect on the performance in terms of lead time. Hence, we insist that the control decision for the non-bottleneck stations should be take into careful consideration for higher system performance.

Table 4. Simulation results

Ruleset case	Lot release	Dispatching for Non-BM	Dispatching for BM	Loading for batch processor	Lead time (hours)	Throughput rate(lots)
Base case	DETERM	FCFS	FCFS	MBS	816.4	728.1
RA1.1	DETERM	FIFO_BM	FCFS	MBS	807.7	733.5
RA1.2	DETERM	SRPT_BM	FCFS	MBS	799.4	729.5
RA2.1	DETERM	FCFS	FIFO_BM	MBS	817.0	732.2
RA2.2	DETERM	FCFS	SRPT_BM	MBS	809.6	728.2
RA2.3	DETERM	FCFS	LOOP_LVL	MBS	811.0	729.2

Conclusions

This paper examines the performance of operational control strategies in semiconductor wafer fab. We present shop floor control schemes where the status of bottleneck stations is considered. Simulation experiments are carried out to evaluate the performance of the various control schemes. From the simulation experiments, we find some interesting insights on the effect of the operational control decisions on the system performance. We have seen that some experimental results are contradictory to the previous findings. These contradictory results should be more studied with various manufacturing settings. This paper can be improved by considering such issues as sequence-dependent setups, multiple products with due dates, make-to-order manufacturing. In addition, the studies with different system configurations with different sizes are recommended to have practical insight.

Acknowledgments—This research was supported by Basic Science research program through the National Research Foundation of Korea (NRF) funded by the Ministry of Education, Science and Technology (2012R1A1A4A01014897).

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